CLAIM AMENDMENTS

1. (currently amended) A method for fine synchronization of a digital telecommunication receiver, comprising a code tracking process for maintaining fine alignment between an incoming spread spectrum signal and a locally generated code, said method comprising: [[-]]

storing a plurality of consecutive samples [[(E-1, E, M, L, Li-1)]] of said incoming spread spectrum signal in a delay line [[(56)]]; [[-]]

determining by interpolation between consecutive samples of said incoming spread spectrum signal, by means of a first [[(26)]] digitally controlled interpolator, an interpolated early sample [[(e)]] anticipating an optimal sampling time instant; [[-]]

determining by interpolation between consecutive samples of said incoming spread spectrum signal, by means of a second [[(24)]] digitally controlled interpolator, an interpolated middle sample [[(m)]] corresponding to said optimal sampling time instant; [[-]]

determining by interpolation between consecutive samples of said incoming spread spectrum signal, by means of a third [[(28)]] digitally controlled interpolator, an interpolated late sample [[(1)]] delayed with respect to said optimal sampling time instant; [[-]]

calculating an error signal [[(4)]] as the difference between the energy of the symbols computed from said interpolated early [[(e)]] and late [[(1)]] samples; [[-]] and

generating, from said error signal [[(a)]], a control signal [[(SouT)]] for controlling the interpolation phase of said second digitally controlled interpolator [[(24)]]; ~~characterised in that said~~

wherein the step of generating a control signal [[(S_{out})]] comprises: [[-]]

extracting the sign of said error signal [[(ξ)]]; [[-]]

accumulating said sign of said error signal [[(ξ)]] for the generation of an intermediate control signal [[(S_M)]]; [[-]]

calculating the absolute value [[(|ξ|]] of said error signal [[(ξ)]] at a time instant n; [[-]]

comparing said absolute value [[(|ξ(n)|)]] of said error signal [[(ξ)]] at said time instant n with the absolute value [[(|ξ(n −1)|]] of said error signal [[(ξ)]] at a previous time instant n-1; [[-]] and

updating said control signal [[(S_{out})]] to the value of said intermediate control signal [[(S_M)]] if the absolute value [[(|ξ(n)|)]] of said error signal at time n is smaller than the absolute value [[(|ξ(n-1)|)]] of the same error signal at time n-1, maintaining otherwise unchanged the value of said control signal [[(S_{out})]].

2. (currently amended) The [[A]] method according to claim 1, wherein said step of accumulating said sign of said error signal [[(ξ)]] provides that the value accumulated has a positive saturation value of +4 and a negative saturation value of -4.

3. (currently amended) The [[A]] method according to claim 1, wherein said step of comparing said absolute value [[(|ξ|)]] of said error signal [[(ξ)]] comprises: [[-]]

storing the absolute value [[(|ξ(n-1)|)]] of said error signal [[(ξ)]] in a first register [[(72)]], maintaining such absolute value [[(|ξ(n-1)|)]] in said register [[(72)]] at least until a new absolute value [[(|ξ(n)|)]] of said error signal [[(ξ)]] has been calculated; [[-]] and

comparing said new absolute value [[(|ξ(n)|)]] of said error signal [[(ξ)]] with the absolute value [[(|ξ(n-1)|)]] stored in said first register [[(72)]], and storing said new absolute value [[(|ξ(n)|)]] in said first register [[(72)]], overwriting the absolute value [[(|ξ(n-1)|)]] previously stored.

4. (currently amended) The [[A]] method according to claim 1, wherein said step of updating said control signal [[(S_{out})]] comprises: [[-]]

storing the value of a previous control signal [[(S_{out}(n-1))]] in a second register [[(78)]], maintaining such value in said

second register [[(78)]] at least until a new value of said intermediate control signal [[(S_M)]] has been calculated; [[-]] and

overwriting the value of said control signal [[(S_{out}(n))]] stored in said second register [[(78)]] with the new value of said intermediate control signal [[(S_M)]] if the absolute value [[(|ξ(n)|)]] of said error signal at time n is smaller than the absolute value [[(|ξ(n-1)|)]] of the same error signal at time n-1, maintaining otherwise unchanged the value stored in said second register [[(78)]].

5. (currently amended) A digital communication receiver comprising a device for maintaining fine alignment between an incoming spread spectrum signal and a locally generated code, said device comprising: [[-]]

a delay line [[(56)]] for storing a plurality of consecutive samples [[(E-1, E, M, L, L+1)]] of said incoming spread spectrum signal; [[-]]

a first digitally controlled interpolator [[(26)]] for determining by interpolation between consecutive samples stored in said delay line [[(56)]] an interpolated early sample [[(e)]] anticipating an optimal sampling time instant; [[-]]

a second digitally controlled interpolator [[(24)]] for determining by interpolation between consecutive samples stored in said delay line [[(56)]] an interpolated middle sample [[(m)]] corresponding to said optimal sampling time instant; [[-]]

a third digitally controlled interpolator [[(28)]] for determining by interpolation between consecutive samples stored in said delay line [[(56)]] an interpolated late sample [[(1)]] delayed with respect to said optimal sampling time instant; [[-]]

at least [[a]] one correlator [[(30, 32, 22)]] for calculating an error signal [[(ξ)]] as the difference between the energy of the symbols computed from said interpolated early [[(e)]] and late [[(1)]] samples; [[-]] and

a circuit for generating a control signal [[(S_{out})]] for controlling the interpolation phase of said second digitally controlled interpolator [[(24)]]; ~~characterised in that said~~ wherein the means for generating a control signal [[(S_{out})]] comprises: [[-]]

a circuit [[(23)]] for extracting the sign of said error signal [[(ξ)]]; [[-]]

a circuit [[(66)]] for accumulating said sign of said error signal [[(ξ)]] in a register, for the generation of an intermediate control signal [[(S_M)]]; [[-]]

a circuit [[(70)]] for calculating the absolute value [[($|\xi(n)|$)]] of said error signal [[(ξ)]] at a time instant n; [[-]]

at least a comparator [[(72, 74)]] for comparing said absolute value [[($|\xi|$)]] of said error signal [[(ξ)]] at said time instant n with the absolute value [[($|\xi(n-1)|$)]] of said error signal [[(ξ)]] at a previous time instant n-1; [[-]] and

a controllable switch [[(76, 78)]] for updating said control signal [[(S_{out})]] to the value of said intermediate control signal [[(S_N)]] if the absolute value [[(|ξ(n)|)]] of said error signal at time n is smaller than the absolute value [[(|ξ(n-1)|)]] of the same error signal at time n-1, maintaining otherwise unchanged the value of said control signal [[(S_{out})]].

6. (currently amended) The [[A]] digital communication receiver according to claim 5, wherein said register in which is accumulated the sign of said error signal [[(ξ)]] has a positive saturation value of +4 and a negative saturation value of -4.

7. (currently amended) The [[A]] digital communication receiver according to claim 5, wherein said at least one comparator [[(72, 74)]] for comparing said absolute value [[(|ξ(n)|)]] of said error signal [[(ξ)]] comprises: [[-]]

a first register [[(72)]] for storing the absolute value [[(|ξ(n-1)|)]] of said error signal [[(ξ)]] at a time instant n-1, maintaining such absolute value [[(|ξ(n-1)|)]] in said register [[(72)]] at least until a new absolute value [[(|ξ(n)|)]] of said error signal [[(ξ)]] has been calculated; [[-]] and

a comparator [[(74)]] for comparing said new absolute value [[(|ξ|)]] of said error signal [[(ξ)]] with the absolute value [[(|ξ(n-1)|)]] stored in said first register [[(72)]], generating a signal [[(C_{out})]] indicating whether said new absolute value

[[($|\xi(n)|$)]] is smaller than the previously stored absolute value [[($|\xi(n-1)|$)]].

8. (currently amended) The [[A]] digital communication receiver according to claim 7, wherein said controllable switch [[(76, 78)]] for updating said control signal [[(S_{out})]] comprises: [[-]]

a second register [[(78)]] for storing the value of a previous control signal [[($S_{out}(n-1)$)]] , maintaining such value in said register [[(78)]] at least until a new value of said intermediate control signal [[(S_M)]] has been calculated; [[-]] and

a switch [[(76)]], controlled by the signal [[(C_{out})]] generated by said comparator [[(74)]], for storing in said second register [[(78)]] a new value of said control signal [[($S_{out}(n)$)]], if said new absolute value [[($|\xi(n)|$)]] is smaller than the previously stored absolute value [[($|\xi(n-1)|$)]], or for leaving unaltered the value stored in the same register [[(78)]] if such condition is not verified.